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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,836	04/12/2004	Sandeep Pant	20-336	1754

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EXAMINER	
WILLOUGHBY, TERRENCE RONIQUE	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,836	PANT ET AL.	
	Examiner	Art Unit	
	Terrence R. Willoughby	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/12/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2-4,7,23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeda et al. (US 6,385,021 B1).

Regarding claim 1, Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit (Fig. 3), comprising: a voltage threshold detector (Fig.3, 37) to detect an electrostatic discharge event wherein a potential is measured between a higher potential power rail (Fig. 3, 48) and a lower potential ground rail (Fig. 3, 43) in excess of a predetermined voltage (column 3, lines 25-35); and a switchable low resistance path (Fig. 3, 40) between said power rail and said ground rail, said low resistance path being adapted to be switched on for a duration of said electrostatic discharge event (column 4, lines 45-49).

Regarding claim 2, Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit according to claim 1, wherein: said low resistance path (Fig. 3, 40) is adapted to be switched ON for significantly longer than 2 microseconds (column 4, lines 45-49 and column 1, lines 56-62).

Regarding claim 3, Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit according to claim 2, wherein: said low resistance path (Fig.

3,40) is adapted to be switched ON for longer than 1000 microseconds (column 1, lines 61-65).

Regarding claim 4, Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit according to claim 2, wherein: said low resistance path (Fig. 3,40) is adapted to be switched ON for longer than 4000 microseconds (column 1, lines 61-65).

Regarding claim 7, Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit according to claim 1, wherein: said low resistance path comprises: a MOSFET transistor (Fig. 3, 40 and column 6, line 4).

Regarding claim 23, Takeda et al. discloses a circuit including an electrostatic shunt circuit (Fig. 3), comprising: a voltage threshold detector (Fig.3, 37) to detect an electrostatic discharge event wherein a potential is measured between a higher potential power rail (Fig. 3, 48) and a lower potential ground rail (Fig. 3, 43) in excess of a predetermined voltage (column 3, lines 25-35); and a switchable low resistance path (Fig. 3, 40) between said power rail and said ground rail, said low resistance path being adapted to be switched on for a duration of said electrostatic discharge event (column 4, lines 45-49).

Regarding claim 24, Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit according to claim 23, wherein: said low resistance path (Fig. 3,40) is adapted to be switched ON for longer than 1000 microseconds (column 1, lines 61-65).

3. Claims 9,10,14,15,19 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (US 6,552,886 B1).

Regarding claim 9, Wu et al. discloses the claimed said integrated circuit (Fig. 4), a power distribution system comprising: a power rail (Vcc); a ground rail (Vss); and an electrostatic discharge shunt connected between said power rail and said ground rail (abstract, lines 1-2), said electrostatic discharge shunt being capable of causing a low resistance path (Fig. 4, 30) to be turned on between said power rail and said ground rail for an entire duration (column 4, lines 52-60) when a potential of said power rail becomes greater than a potential of said ground rail by more than a predetermined threshold (abstract).

Regarding claim 10, Wu et al. discloses the claimed said integrated circuit according to claim 9, wherein said integrated circuit is based on 3.3 v technology (Fig. 5).

Regarding claim 14, Wu et al. discloses the claimed said integrated circuit according to claim 9, wherein said low resistance path comprises: a MOSFET transistor (Fig. 4, 30).

Regarding claim 15, Wu et al. discloses the claimed said method of providing robustness to an electrical circuit from an electrostatic discharge event, said method comprising: detecting an ESD condition wherein a potential of a power rail of said electrical circuit becomes greater than a potential of a ground rail of said electrical circuit by more than a predetermined threshold; and turning ON a low resistance path

between said power rail and said ground rail for a duration of an occurrence of said detected ESD condition.

Regarding claim 19, Wu et al. discloses the claimed said apparatus for providing robustness to an electrical circuit from an electrostatic discharge event, comprising: a means for detecting an ESD condition wherein a potential of power rail (Vcc) of said electrical circuit becomes greater than a potential of a ground rail (Vss) of said electrical circuit by more than a predetermined threshold (abstract); and a means for turning ON a low resistance path (Fig. 4, 30) between said power rail and said ground rail for a duration of an occurrence of said detected ESD condition (column 4, lines 52-60).

4. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al. (US 6,385,021 B1) and further in view of Wu et al. (6,552,886 B1).

Regarding claim 5, Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit according to claim 1 above, however Takeda et al. does not disclose said a driver between said voltage threshold detector and said switchable low resistance path.

However, Wu et al. discloses a driver (Fig. 4,34 and 36) between said voltage threshold detector (Fig. 4, 32 and 38) and said switchable low resistance path (Fig. 4,30). It would have been obvious to those skilled in the art at the time the invention was made to have modified the electrostatic discharge circuit of Takeda et al. by providing a driver stage between said voltage threshold detector and said switchable low resistance

path taught by Wu et al. to extend the discharge time that the clamping transistor is shunting current during the electrostatic discharge pulse.

Regarding claim 6, Takeda et al. in view of Wu et al. discloses the claimed said electrostatic shunt circuit according to claim 5, wherein said driver comprises a series connection of a plurality of inverters (Fig. 4, elements 32,34,36, and 38).

5. Claims 11,16, 20 are rejected under 35 U.S.C. 103(a) as being obvious over Wu et al. (US 6,552,886 B1).

Regarding claim 11, Wu et al. discloses the claimed said integrated circuit according to claim 9, however Wu et al. does not disclose the said predetermined threshold to be at least 5 volts, however, it would have been obvious to those skilled in the art at the time the invention was made to configure the desired threshold based the predetermined fraction of the voltage divider (24,25) being used in Wu et al. circuit to bias the electrostatic pulse of the clamping transistor. Furthermore, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 16, Wu et al. discloses the claimed said method of providing robustness to an electrical circuit from an electrostatic discharge event according to claim 15, however Wu et al. does not disclose the said predetermined threshold to be at least 5 volts, however, it would have been obvious to those skilled in the art at the time the invention was made to configure the desired threshold based the predetermined fraction of the voltage divider (24,25) being used in Wu et al. circuit to bias the electrostatic pulse of the clamping transistor. Furthermore, since it has been held that

discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 20, Wu et al. discloses the claimed said apparatus for providing robustness to an electrical circuit from an electrostatic discharge event according to claim 19, however Wu et al. does not disclose the said predetermined threshold to be at least 5 volts, however, it would have been obvious to those skilled in the art at the time the invention was made to configure the desired threshold based the predetermined fraction of the voltage divider (24,25) being used in Wu et al. to bias the electrostatic pulse of the clamping transistor. Furthermore, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 21, Wu et al. discloses the claimed said apparatus for providing robustness to an electrical circuit from an electrostatic discharge event according to claim 19 above, however Wu et al. does not disclose the said low resistance path is adapted to be switched ON for significantly longer than 2 microseconds.

6. Claims 12,13,17,18,21,22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 6,552,866 B1) and further in view of Takeda et al. (6,385,021 B1).

Regarding claim 12, Wu et al. discloses the claimed said integrated circuit according to claim 9, wherein: said low resistance path (Fig. 4, 30) is adapted to be switched on for a period of time during a electrostatic event (column 4, lines 56-60),

however Wu et al. does not disclose the said low resistance path is adapted to be switched ON for significantly longer than 2 microseconds.

However, Takeda et al. disclose a low resistance path (Fig. 3, 40) adapted to be switched ON for significantly longer than 2 microseconds for an electrostatic discharge protection circuit (column 4, lines 45-52). It would have been obvious to those skilled in the art at the time the invention was made to have modified the integrated circuit of Wu et al. by providing a low resistance path adapted to be switched ON for the duration of the electrostatic discharge event taught by Takeda et al. to provide a more accurate and controllable electrostatic discharge protection of the core circuitry and special protection for noise immunity at the power-up of the circuitry.

Regarding claim 13, Wu et al. in view of Takeda et al. discloses an integrated circuit including an electrostatic shunt circuit according to claim 12, wherein: said low resistance path (Takeda et al., Fig. 3,40) is adapted to be switched ON for longer than 1000 microseconds (Takeda et al., column 1, lines 61-65).

Regarding claim 17, Wu et al. in view of Takeda et al. discloses the claimed said method of providing robustness to an electrical circuit from an electrostatic discharge event according to claim 15, wherein: said low resistance path is adapted to be switched ON for significantly longer than 2 microseconds (Takeda et al., column 4, lines 45-52).

Regarding claim 18, Wu et al. in view of Takeda et al. disclose the claimed said method of providing robustness to an electrical circuit from an electrostatic discharge

event according to claim 17, wherein: said low resistance path is adapted to be switched ON for longer than 1000 microseconds (Takeda et al., column 1, lines 61-65).

Regarding claim 21, Wu et al. in view of Takeda et al. discloses the claimed said apparatus for providing robustness to an electrical circuit from an electrostatic discharge event according to claim 19, wherein: said low resistance path is adapted to be switched ON for significantly longer than 2 microseconds (Takeda et al., column 4, lines 45-52).

Regarding claim 22, Wu et al. in view of Takeda et al. discloses the claimed said apparatus for providing robustness to an electrical circuit from an electrostatic discharge event according to claim 21, wherein: said low resistance path is adapted to be switched ON for significantly longer than 1000 microseconds (Takeda et al., column 4, lines 45-52).

7. Claims 8 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al. (US 6,385,021 B1) and further in view of Whitney et al. (US 2002/0024791 A1).

Regarding claim 8, Takeda et al. discloses the claimed said electrostatic shunt circuit according to claim 1 and 23 above, however, Takeda et al. does not disclose said integrated circuit includes an Firewire IEEE 1394 interface.

However, Whitney et al. discloses an electrostatic shunt circuit (page 1, paragraph [0002]) to protect an integrated circuit including a Firewire IEEE 1394 interface (Fig. 13A and 13B and page 6, paragraph [0093], lines 1-4). It would have been obvious to those skilled in the art the at the time the invention was made to

provide the Firewire IEEE 1394 interface taught by Whitney et al. to the electrostatic shunt circuit taught by Takeda et al. to protect the input and output signals and to improve accessibility of the connections to the transmission lines and other lines of data transfer interfaces.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRW
1/26/06

PHUONG T VU
PRIMARY EXAMINER